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Comparison of CMOS Current Mirror Sources

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***Abstract*— The benefits of using good current sources in analog signal conditioning circuit are well known. The objectives of this paper are to built and compare the CMOS current mirror sources fit for the desired applications. The current sources are developed by using current mirror circuits fed from identical input current source. A straightforward approach to design and compare the current sources based on four parameters is presented here. The current mirror, Cascode current mirror and Wilson current mirror sources are compared with output resistance, systematic gain error, input voltage and minimum output voltage. The simulation results are included in the paper and validated with the derived values. The proposed current sources circuits have designed in 0.25µm CMOS technology with the help of EDA tool Tanner V14.1.**

***Keywords*- Current mirror; cascode current mirror; output resistance; Wilson current mirror; aspect ratio.**

I. Introduction

Current mirrors using MOSFETs have been widely used in analog integrated circuits both as biasing elements and as active loads for amplifier stages [3] [9]. The current mirrors as biasing circuits result in circuit performance insensitive to variations in power supply, temperature and presence of common mode noise [4] [5]. In MOS, circuits bias current is small, then use of current mirrors becomes economical than resistors in terms of the die area required. For low power supply amplifiers, high voltage gain is obtained using current mirror as a load by offering high incremental resistance [2].

A current mirror is an element with at least three terminals (IN, OUT, COMMON) as shown in Fig. 1. The power supply is applied to common terminal and input current source is applied to input terminal [1]. The output current comes out to be equal to the input current multiplied by current gain. If this current gain is unity, the input current reflects at output terminal and the circuit named as current mirror. Ideally, the current mirror gain is independent of input frequency, and the output current is independent of potential between output and common terminal. The voltage between input and common terminal is ideally required to be zero, as this allows the entire supply voltage to drop across input current source. Some times more than one input and or output terminals are used.

Practically MOS current mirrors deviate from this ideal behavior. The deviations from ideal conditions are as follows.

1. The variation of the current mirror output current with changes in voltage at output terminal is one of the most important deviations. The small signal output resistance, R_o of the current mirror characterizes this effect. This resistance is included in Norton-equivalent model at the output. The R_o directly affects the performance of circuits that use current mirrors. Higher value

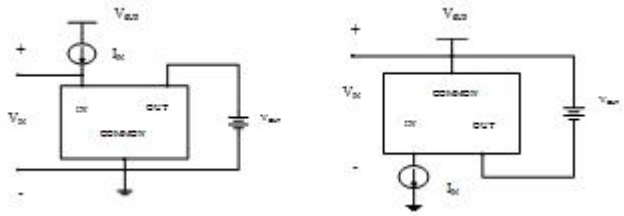

Fig. 1. Current mirror block diagram with reference to ground and power supply.

of R_o is achieved when the output current decreases. This alsodecreases the maximum operating speed [7].

2. The gain error, which is deviation of gain of current mirror from its desired value, is another error source. The gain error comprises of the systematic gain error and the random gain error. The systematic gain error ε, is the gain error caused even if all matched elements in the mirror are perfectly matched. The unintended mismatches between matched elements cause random gain error.

3. The voltage available across the input current source is reduced due to a positive voltage drop (V_{IN}) created by current source connected to input. Low V_{IN} simplifies the design of input current source.

4. The output current depends mainly on the input current if the output voltage V_{OUT} is positive. This output voltage is limited to a minimum value (V_{OUTmin}) that allows the output device to operate in saturation. Minimizing V_{OUTmin} maximizes the range of output voltages for which the current mirror output resistance is almost constant.

In this paper, the performances of various current mirrors are compared to each other for above four parameters: R_o, ε, V_{IN} and V_{OUTmin}.

II. Types of Current Sources

A. A Simple MOS Current Mirror

Fig. 2 shows a simple current mirror using MOSFETs.The drain of M_1 is shorted with gate, therefore, the channel does not exist at the drain. Thus operates in the saturation of active region if threshold voltage is positive [7]. The M_1 is said to diode connected. Let assume that M_2 also operates in active region and both M_1 and M_2 have infinite output resistance. The drain current of M_2 (I_{D2}) is controlled by V_{GS2} that is equal to V_{GS1}. The gate source voltage of MOSFET is usually separated into the threshold voltage V_t and the overdrive voltage V_{ov}. The overdrive for M_2 assuming square law behavior of MOSFET becomes,

$$V_{OV2} = V_{GS2} - V_t = \sqrt{\frac{2I_{D2}}{k'(W/L)_2}} \quad (1)$$

The transconductance parameter k' is proportional to mobility and the mobility falls with increasing temperature.Hence,

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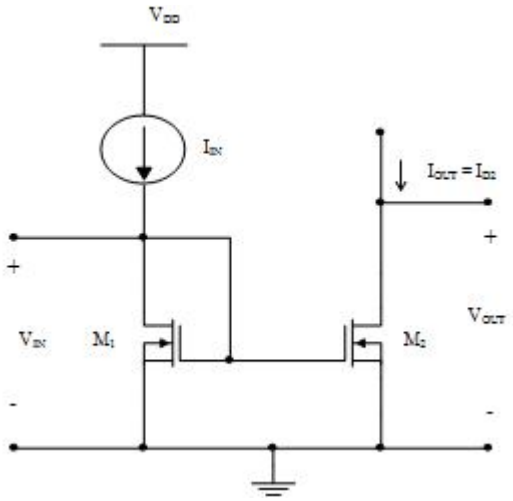

Fig. 2. Simple MOS current mirror

the overdrive rises with rising temperature. Rearranging (1) and equating gate voltages of M_1 and M_2,

$$V_{GS2}=V_t+\sqrt{\frac{2I_{D2}}{k'(W/L)_2}}=V_{GS1}=V_t+\sqrt{\frac{2I_{D1}}{k'(W/L)_1}} \quad (2)$$

Thus, overdrive of M_2 is equal to that of M-$_1$.

$$V_{ov2}=V_{ov1}=V_{ov} \quad (3)$$

If MOSFETs are identical, $(W/L)_2=(W/L)_1$ and therefore,

$$I_{OUT}=I_{D2}=I_{D1} \quad (4)$$

This shows that the current flowing in the drain of M_1 is mirrored to the current flowing in the drain of M_2. As for MOSFETs forward current gain (β_F) tends to ∞, applying KCL at the drain of M_1, (4) becomes

$$I_{OUT}=I_{D1}=I_{IN} \quad (5)$$

Hence, the gain of the current mirror is unity, for identical devices operating in saturation region with infinite output resistance. This result assumes that the gate currents are zero. The result in (5) holds good for dc and low frequency ac currents. The gate currents of M_1 and M_2 increase with increase in input frequency due to finite gate-source capacitance. The part of the input current that flows through the gate does not flow into the drain of M_1. This decrease the gain of current mirror as the frequency of input increases [10].

If the devices are not identical,

$$I_{OUT}=\frac{(W/L)_2}{(W/L)_1}I_{D1}=\frac{(W/L)_2}{(W/L)_1}I_{IN} \quad (6)$$

The aspect ratio of MOSFETs changes, the gain of the current mirror. To change the gain of current mirror, width (W) is changed keeping length (L) constant.

The drain currents of MOSFETs assumed independent of their drain-source voltages in (2). In saturation region, the drain current actually increases slowly with drain-source voltage. The output characteristic of M_2 is as shown in Fig. 3. The output resistance of the current mirror at given operating point is the reciprocal of the slope of the output characteristic at that point.

$$\text{Here, } R_o=r_{o2}=\frac{V_A}{I_{D2}}=\frac{1}{\lambda I_{D2}} \quad (7)$$

where, V_A is the early voltage and λ the channel-length modulation parameter. At the point shown on the characteristic curve $V_{DS2}=V_{DS1}$ and $V_{GS2}=V_{GS1}$.

If the slope of characteristic curve in saturation region is constant, a straight line passing through the operating point predicts the variation in I_{D2} with V_{DS2}. Therefore,

$$I_{OUT}=\frac{(W/L)_2}{(W/L)_1}I_{IN}\left(1+\frac{V_{DS2}-V_{DS1}}{V_A}\right) \quad (8)$$

The ideal gain of current mirror is $(W/L)_2/(W/L)_1$. Then from (8) the systematic gain error, ε is given as,

$$\varepsilon=\frac{V_{DS2}-V_{DS1}}{V_A} \quad (9)$$

In the input voltage for MOS current mirror (V_{IN}) is given as,

$$V_{IN}=V_{GS1}=V_t+V_{ov1}=V_t+V_{ov} \quad (10)$$

According to square law behavior of MOSFET, the overdrive voltage is proportional to square root of the input current.

The minimum output voltage required to keep M_2 in saturation is,

$$V_{OUTmin}=V_{ov2}=V_{ov}=\sqrt{\frac{2I_{OUT}}{k'(W/L)_2}} \quad (11)$$

V_{OUTmin} can be made arbitrarily small as it depends on device geometry. If MOSFETs operate in weak inversion, then V_{OUTmin} becomes

$$V_{OUTmin}=3V_T \quad (12)$$

Here V_T is thermal voltage.

B. Cascode Current Mirror

One of the desirable characteristic for a current mirror is a very high output resistance that can be achieved by cascode connection [6]. A MOSFET current mirror based on cascode connection is shown in Fig. 4. The MOSFETs M_1 and M_3 form a simple current mirror. M_2 acts as the common gate part of the cascode and transfers the drain current of M_1 to the output presenting a high output resistance. M_4 acts as a diode level shifter and assures that M_2 and M_1 always remain in saturation.

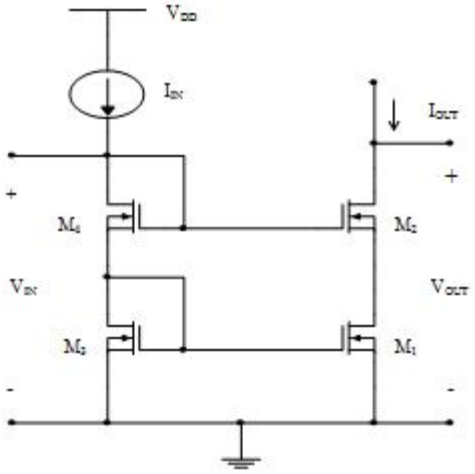

Fig. 3. MOS cascode current mirror

The small signal output resistance of M_2 in common gate configuration, with r_{o1} as a source resistance is given in terms of small signal parameters as,

$$R_o=r_{o2}\left[1+(g_{m2}+g_{mb2})r_{o1}\right]+r_{o1} \quad (13)$$

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For MOS cascode as dc current gain β_0-- ∞, the number of stacked cascode devices can be increased. This will be limited by the MOS substrate leakage current that creates a resistive shunt dominating output resistance for $V_{OUT}>V_{OUTmin.}$

Applying KVL in Fig. 4,

$$V_{DS1}=V_{GS3}+V_{GS4}-V_{GS2} \quad (14)$$

As $V_{DS3}=V_{GS3}$, (14) shows that $V_{DS1}=V_{DS3}$ when $V_{GS2}=V_{GS4}$. With this condition, the systematic current gain of the cascode current mirror is zero due to identical bias on M_1 and M_2 and β_F ∞. Actually V_{GS2} is not exactly equal to V_{GS4} even with perfectly matched MOSFETs unless $V_{OUT}=V_{IN}$. Thus, V_{DS1} V_{DS3} and leads to,

$$\varepsilon \simeq 0 \quad (15)$$

The input voltage of this MOS cascode mirror is,

$$V_{IN}=V_{GS3}+V_{GS4}$$

$$=V_{t3}+V_{ov3}+V_{t4}+V_{ov4}$$

The input voltage here is composed of two gate-source drops, each including threshold and overdrive components. Neglecting body effect and assuming that MOSFETs have got equal overdrives,

$$V_{IN} = 2V_t + 2V_{ov} \quad (16)$$

Addition of further cascode levels increases the input voltage by another threshold and another overdrive component per cascode. This fact increases the difficulty of designing the input current source with low power supply voltages.When both M_1 and M_2 operate in saturation region, V_{DS1} $V_{DS3}=V_{GS3}$.To operate M_2 in saturation it is required that $V_{DS2}>V_{OV2}$. Hence, minimum output voltage for which M_1 and M_2 operate in saturation region is, $V_{OUTmin}=V_{DS1}+V_{ov2}$

$$\simeq V_{GS3}+V_{ov2}=V_t+V_{ov3}+V_{ov2} \quad (17)$$

If all MOSFETs have identical overdrives, $V_{OUTmin} = V_t + 2V_{ov}$

If $V_{OUT} < V_{OUTmin}$, M_2 operates in the triode region and if $V_{OUT} < V_{ov1}$, both M_1 and M_2 operate in the triode region. Even if the overdrive in (18) is made small by using larger W, the threshold term remains that represent significant loss of voltage swing [8].

A. Wilson current mirror

The Wilson current mirror is as shown in Fig. 5. Let consider the circuit without M_4.This circuit uses negative feedback through M_1 and activates M_3 to raise the output resistance. A feedback path is formed that regulates I_{d3} so that it equals the input current. To find the output resistance of the Wilson current mirror when all MOSFETs operate in saturation, the small- signal model is used. Applying a test mirror comes out to be,

$$R_o=\frac{1}{g_{m1}}+r_{o2}+g_{m2}r_{o2}\left(2+\frac{1}{g_{m1}r_{o3}}\right)r_{o3} \quad (18)$$

$$\simeq (2+g_{m2}r_{o3})r_{o2}$$

The calculation of R_o ignores body effect. The body effect of M_2 has little effect on R_o because M_1 is diode connected, the voltage from source of M_2 to ground is almost constant.

The systematic gain error here is not zero even if $\beta_F \rightarrow \infty$, as the drain source voltage of M_3 differs from that of M_1 by the gate source voltage of M_2. Thus without M_4,

$$\varepsilon=\frac{V_{DS1}-V_{DS3}}{V_A}=-\frac{V_{GS2}}{V_A} \quad (19)$$

When M_4 is inserted in series with M_3, it equalizes the drain source voltages of M_3 and M_1. Then, $\varepsilon \simeq 0$.

The output resistance is still given by (18), if all MOSFETs operate in saturation. Insertion of M_4 does not change the minimum output voltage or input voltage. The minimum output voltage ignoring body effect and assuming equal overdrives is,

$$V_{OUTmin}=V_{GS1}+V_{ov2}=V_t+2V_{ov} \quad (20)$$

With this condition the input voltage is

$$V_{IN} = V_{GS1} + V_{GS2} = 2V_t + 2V_{ov} \quad (21)$$

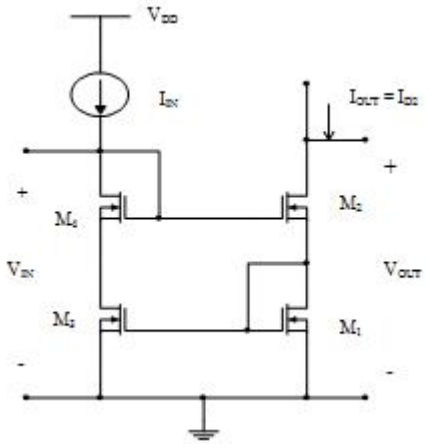

Fig. 4. MOS Wilson current mirror

III. Proposed Circuits

A. MOS Current Mirror

The proposed circuit of MOS current mirror is built selecting NMOS devices M_1 and M_2 of same dimension of aspect ratio 10/0.5 µm/µm. The transconductance (g_m) and output resistance (r_o) of the MOSFETs used are found out using simulation results as 1.2mA/V and 45.43 Ω The response of all the current sources discussed above depends on the current source I_{IN}. The current source I_{IN} used here is a PMOS device maintained in saturation for all operating conditions, with the help of bias applied on gate V_b. The current supplied by I_{IN} is maintained 365µA with the help of bias V_b on gate of PMOS device M_3. The PMOS device M_3 is selected with aspect ratio 5/0.5 µm/µm and gate bias V_b required is 0.6639V. The supply voltage selected is 2.5V. The gate bias 0.6639V is obtained from supply voltage 2.5V using voltage reference circuit made up of one PMOS and one NMOS device of aspect ratio 3/0.5µm/µm and 18.85/0.5µm/µm respectively[11]. The similar reference voltage circuit is used in all proposed circuits.The output characteristic of MOS current mirror source is as shown in Fig. 6. The MOSFET M_2 is seen to be in triode region for $V_{DS2} < 0.7V$ and enters saturation region thereafter. The output resistance R_o calculated from output characteristic curve comes out to be 47.34k. Ω The minimum output voltage for which M_2 remains in saturation is 0.7 approximately equal to overdrive of MOSFET. The load resistance R_L is connected at the drain of M_2. The output voltage and output current readings are obtained by varying R_L.

B.Cascode Current Source

The proposed cascode current mirror source is as shown in Fig.

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7. The aspect ratio dimensions of NMOS devices M_1-M_4 is kept same to be 10/0.5µm/µm.

The dimension of current source PMOS device M_5 is also kept same 5/0.5 µm/µm and to get the current of 365µA, V_b now required comes out to be 0.1996V. This required voltage reference of 0.1996V and is derived from 2.5V V_{DD}

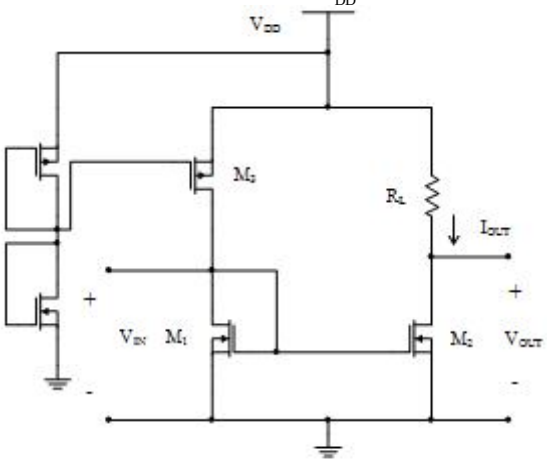

Fig. 5. Proposed MOS current mirror circuit

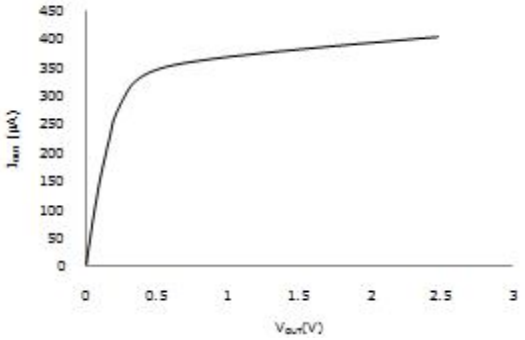

Fig. 6. Output characteristic of MOS current mirror

using a voltage reference circuit as shown in Fig. 7. As the reference voltage is too lower, two PMOS and one NMOS device is required. The PMOS device dimensions comes out to be W/L=0.05/2 µm/µm and NMOS device dimension comes out to be W/L = 61.12/0.5µm/µm. The PMOS devices with small W and large L offer higher resistance and NMOS device with large

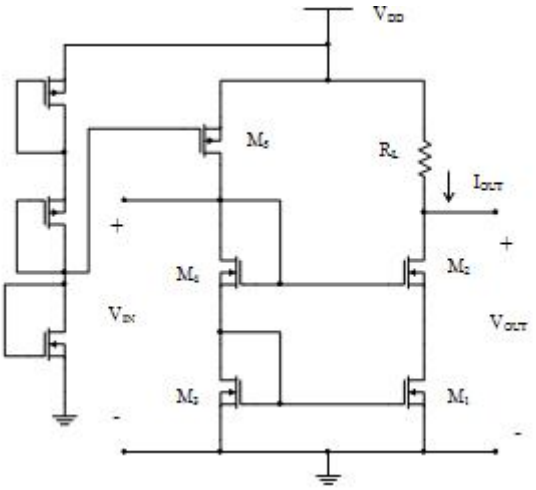

Fig. 7. Proposed MOS cascode current mirror circuit

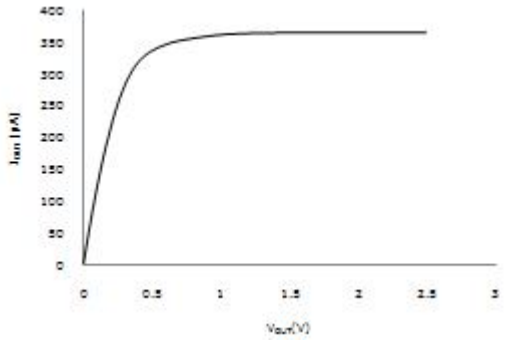

Fig. 8. I-V characteristic of cascode current mirror

W and small L offer lower resistance required for generation of small V_b from large value of V_{DD} [12].

The output resistance measured from the output characteristics curve (Fig. 8) comes out to be 1.622M Ω When output voltage starts to built up, initially M_1 and M_2 operate in triode region. As output voltage increases, M_1 enters into saturation first. With further increase in output voltage, both the devices operate in saturation region. The minimum output voltage required to maintain both devices in saturation comes out to be 1.4V, which is approximately double of the overdrive required for single device.

C. Wilson Current Mirror Source

As the three current sources are to be compared, they must be designed fed from identical current source of 365µA. The aspectratio dimensions of NMOS devices M_1-M_4 is selected to be same 10/0.5µm/µm and the aspect ratio of current source PMOS device M_5 also selected same 5/0.5 µm/µm. To get the current of 365µA from M_5 the gate drive voltage V_b required is 0.2135V. This once again is a lower reference voltage derived from higher V_{DD}.

The reference voltage circuit comes out to be similar as that of cascode current mirror source with dimension of PMOS devices W/L = 0.05/2 µm/µm and dimension of NMOS device W/L = 39.7/0.5 µm/µm as shown in Fig. 9.

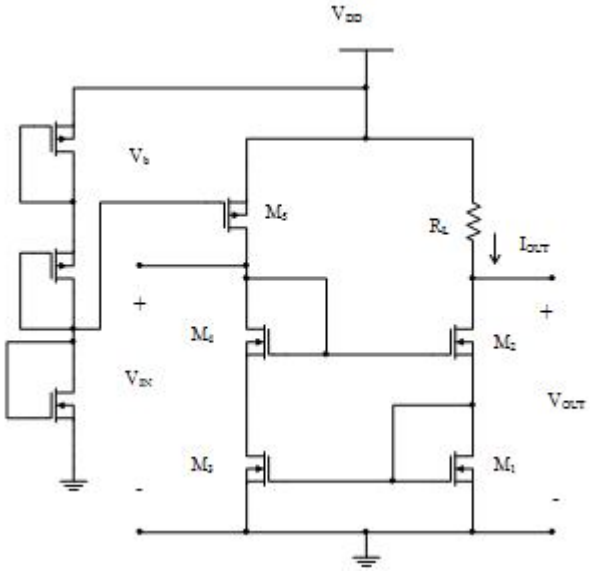

Fig. 9. Proposed MOS Wilson current mirror circuit

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Ω.

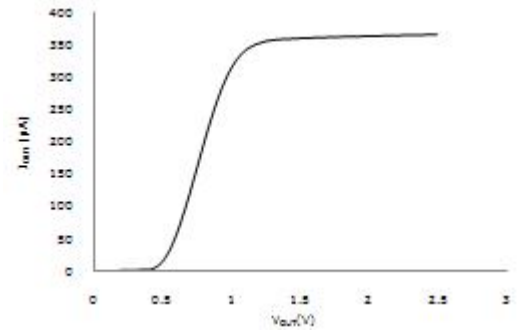

Fig. 10. I-V Characteristic of Wilson current mirror

TABLE I. SUMMARY OF PARAMETERS MEASURED FROM PROPOSED CIRCUITS

Circuits/ Parameters	Simple current mirror	Cascode current mirror	Wilson current mirror
R_o	47.34kΩ	1.622MΩ	1.71MΩ
ε	1.093	1.0045	1.0045
V_{IN}	0.8644	1.8813	1.8734
V_{OUTmin}	0.7V	1.4V	1.94V

CONCLUSION

We have presented a detailed analysis of three current mirror sources. The performance of three sources will be depending on the internal current source used (I_{IN}). The internal current source is built up of PMOS device having aspect ratio 5/0.5 µm/ µm and output current 365µA. The R_o of Wilson current mirror source comes out to be maximum at the cost of raised minimum output voltage (Table I). The minimum output voltage of simple current mirror comes out to be least and R_o lowered. The operating range of simple current mirror is maximum and that of Wilson current mirror source is minimum. These results show that the simple mirror current source and cascode mirror current source can be used as active load for differential amplifiers, whereas Wilson mirror current source can be used as a bias current source supplying constant current to MOSFET devices in differential amplifiers. The performance of current mirrors can be improved employing more cascoded stages but with increased minimum output voltage.

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